

Obraz zawierający tekst, zrzut ekranu, linia, Czcionka

Opis wygenerowany automatycznie

Testbramki.vhd – KOD

-- Vhdl test bench created from schematic C:\.Xilinx\lab1\Z1.sch - Mon Oct 16 12:19:17 2023

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-- Notes:

-- 1) This testbench template has been automatically generated using types

-- std\_logic and std\_logic\_vector for the ports of the unit under test.

-- Xilinx recommends that these types always be used for the top-level

-- I/O of a design in order to guarantee that the testbench will bind

-- correctly to the timing (post-route) simulation model.

-- 2) To use this template as your testbench, change the filename to any

-- name of your choice with the extension .vhd, and use the "Source->Add"

-- menu in Project Navigator to import the testbench. Then

-- edit the user defined section below, adding code to generate the

-- stimulus for your design.

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LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.numeric\_std.ALL;

LIBRARY UNISIM;

USE UNISIM.Vcomponents.ALL;

ENTITY Z1\_Z1\_sch\_tb IS

END Z1\_Z1\_sch\_tb;

ARCHITECTURE behavioral OF Z1\_Z1\_sch\_tb IS

COMPONENT Z1

PORT( X : IN STD\_LOGIC\_VECTOR (3 DOWNTO 0);

Y : OUT STD\_LOGIC\_VECTOR (3 DOWNTO 0));

END COMPONENT;

SIGNAL X : STD\_LOGIC\_VECTOR (3 DOWNTO 0);

SIGNAL Y : STD\_LOGIC\_VECTOR (3 DOWNTO 0);

BEGIN

UUT: Z1 PORT MAP(

X => X,

Y => Y

);

X <= "0000", "0001" after 100ns, "0010" after 200ns, "0011" after 300ns, "0100" after 400ns,

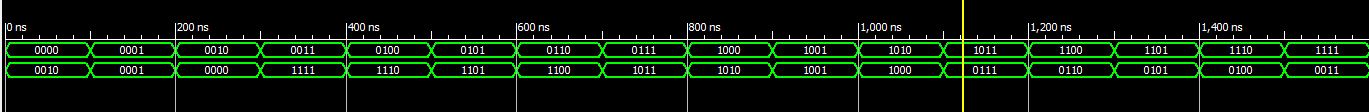
"0101" after 500ns, "0110" after 600ns, "0111" after 700ns, "1000" after 800ns, "1001" after 900ns,

"1010" after 1000ns, "1011" after 1100ns, "1100" after 1200ns, "1101" after 1300ns, "1110" after 1400ns,

"1111" after 1500ns;

END;

Symulacja Bechawioralna:



Tu że możemy poszczególne sygnały śledzić w behawioralnej:  
Obraz zawierający zrzut ekranu, oprogramowanie, linia, Oprogramowanie multimedialne

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Post fit symulacja

Obraz zawierający oprogramowanie, Oprogramowanie multimedialne, Oprogramowanie graficzne, linia

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